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# TRANSMITTAL FORM

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Total Number of Pages In This Submission

111

Application Number 10/086,980  
Filing Date 03/01/2002  
First Named Inventor Kent  
Art Unit 2676  
Examiner Name Tung, Kee M.  
Attorney Docket Number TD-168

## ENCLOSURES (Check all that apply)

<input checked="" type="checkbox"/> Fee Transmittal Form <input checked="" type="checkbox"/> Fee Attached <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s) <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement  <input type="checkbox"/> Certified Copy of Priority Document(s) <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input checked="" type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address <input type="checkbox"/> Terminal Disclaimer <input type="checkbox"/> Request for Refund <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences <input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief) <input type="checkbox"/> Proprietary Information <input type="checkbox"/> Status Letter <input type="checkbox"/> Other Enclosure(s) (please identify below):
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Printed name	David W. Roe		
Date	03/04/2005	Reg. No.	55,785

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Typed or printed name	Peggy Heath	Date	03/04/2005

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**FEE TRANSMITTAL**  
**For FY 2005**☐ Applicant claims small entity status. See 37 CFR 1.27**TOTAL AMOUNT OF PAYMENT** (\$) 500.00**Complete if Known**

Application Number 10/086,980

Filing Date 03/01/2002

First Named Inventor Kent, Osman

Examiner Name Tung, Kee M.

Art Unit 2676

Attorney Docket No. TD-168

**METHOD OF PAYMENT (check all that apply)**☒ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): \_\_\_\_\_☒ Deposit Account Deposit Account Number: 07-2320 Deposit Account Name: Groover & Holmes

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☐ Charge fee(s) indicated below☐ Charge fee(s) indicated below, except for the filing fee☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17☒ Credit any overpayments**WARNING:** Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.**FEE CALCULATION****1. BASIC FILING, SEARCH, AND EXAMINATION FEES**

Application Type	FILING FEES		SEARCH FEES		EXAMINATION FEES		Fees Paid (\$)
	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	Fee (\$)	Small Entity Fee (\$)	
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

**2. EXCESS CLAIM FEES****Fee Description**

Each claim over 20 (including Reissues)

Fee (\$)	Small Entity Fee (\$)
50	25
200	100
360	180

Each independent claim over 3 (including Reissues)

Multiple dependent claims

**Total Claims**      **Extra Claims**      **Fee (\$)**      **Fee Paid (\$)**

- 20 or HP = \_\_\_\_\_ x \_\_\_\_\_ = \_\_\_\_\_

HP = highest number of total claims paid for, if greater than 20.

**Indep. Claims**      **Extra Claims**      **Fee (\$)**      **Fee Paid (\$)**

- 3 or HP = \_\_\_\_\_ x \_\_\_\_\_ = \_\_\_\_\_

HP = highest number of independent claims paid for, if greater than 3.

**Multiple Dependent Claims**  
**Fee (\$)**      **Fee Paid (\$)****3. APPLICATION SIZE FEE**

If the specification and drawings exceed 100 sheets of paper (excluding electronically filed sequence or computer listings under 37 CFR 1.52(e)), the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

**Total Sheets**      **Extra Sheets**      **Number of each additional 50 or fraction thereof**      **Fee (\$)**      **Fee Paid (\$)**

- 100 = \_\_\_\_\_ / 50 = \_\_\_\_\_ (round up to a whole number) x \_\_\_\_\_ = \_\_\_\_\_

**4. OTHER FEE(S)**

Non-English Specification, \$130 fee (no small entity discount)

Other (e.g., late filing surcharge): Appeal Brief

**Fees Paid (\$)**

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**SUBMITTED BY**

Signature		Registration No. (Attorney/Agent) 55,785	Telephone 972-980-5840
Name (Print/Type)	David W. Roe		Date 03/04/2005

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In the United States Patent and Trademark Office

In re application of: :  
Kent, Osman : Art Unit: 2676  
AN 10/086,980 : Examiner: Tung, Kee M.  
Filed: 03/01/2002 : Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (As Amended)

APPEAL BRIEF

Honorable Commissioner of Patents and Trademarks  
Alexandria, VA 22313

Sir:

Enclosed is an Appeal Brief with four Appendices (including a copy of the Notice of Appeal previously filed). Docketing for Oral Argument is requested. Four complete copies are included, three bound and one unbound.

Any extension of time necessary for consideration of this appeal is also hereby requested. The correct amount of fee is believed to be as follows, and a check for this amount is enclosed. Please charge any underpayment, or credit any overpayment, to Deposit Account Number 07-2320.

03/14/2005 CCHAU1 00000034 10086980

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APPENDIX A - Text of Claims on Appeal

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APPENDIX C - Copy of Notice of Appeal previously filed

APPENDIX D - Copy of application drawings

## Table of Authorities

### Cases

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**Real Party in Interest**

The real party in interest, and assignee of this case, is *3Dlabs Inc., Ltd.*, of Reid Hall, Hamilton HM11, Bermuda.

**Related Appeals and Interferences**

To the best knowledge and belief of the undersigned attorney, there are no related appeals or interferences.

**Status of Claims**

Claims 1, 3-5 and 7-35 are pending and are each under final rejection. No other claims are pending. Each claim is appealed.

**Status of Amendments after Final**

An amendment after final rejection was submitted on October 8, 2004. This amendment was not entered.

## Summary of Invention

The following summary refers to disclosed embodiments and their advantages, but does not delimit any of the claimed inventions.

The present invention relates to complex integrated circuits, particularly parallelized graphics accelerators. (Page 1, lines 3-4)

The only practical way to design high performance graphics chips involves replicating part of the design (i.e. multiple texture pipes) so that multiple operations can be carried out in parallel. (Page 3, lines 8-10)

As the size of the silicon die is large the expected yield from manufacturing is less than desirable. (Page 3, lines 10-12) During testing a single bit error anywhere on the die will force that die to be scrapped. (Page 3, lines 12-13) The technique of redundancy has been used, particularly in memory chips, whereby extra spare rows of memory cells (or some other element) are designed in and this can be used to replace a row which has an error in it. (Page 3, lines 13-16)

In latest generation graphics chips the replicated parts are too big to have any spares so we do not have the notion of redundancy. (Page 3, lines 17-18) However, by internally reconfiguring the chip we can still make use of a die with one or more failing texture pipes, for example. (Page 3, lines 19-20) This allows us to take die which would otherwise be classified as scrap and use them in a lower performance product. (Page 3, lines 20-22)

To allow this to be implemented we need to have reconfigurability in the architecture, independent scan chains so that a manufacturing fault can be isolated and a method of recording the test result inside the chip. (Page 3, lines 22-25)

This idea can be applied not only to complex chips in the field of graphics, but to any market where large parts of the design are replicated to give scalable performance. (Page 3, lines 26-28)

The disclosed innovations, in various embodiments, provide one or more of at least the following advantages: The ability to use partially defective die as fully functioning part with lower performance, which are marketed and sold at a lower price point, and a reconfigurable chip design wherein performance can be scaled by changing the number of configured units. (Page 4, lines 1-7)



## **Issue**

Are claims 1, 3-5 and 7-35 unpatentable over Baldwin (6,025,853) in view of Brent et al (5,459,864) under 35 U.S.C. 103(a)?

## **Grouping of Claims**

Claims 1, 3-5 and 7-35 are under appeal. Claims 1, 12, 20 and 28 are independent claims. Claims 3-5, and 7-11 are dependant upon claim 1. (Henceforth claim 1 and those claims that depend from claim 1 shall be referred to as “Group A”). All claims of Group A stand or fall together as argued below. Claims 13-19 are dependent upon claim 12. (Henceforth claim 12 and those claims that depend from claim 12 shall be referred to as “Group B”). All claims of Group B stand or fall together as argued below. Claims 21-27 are dependent upon claim 20. (Henceforth claim 20 and those claims that depend from claim 20 shall be referred to as “Group C”). All claims of Group C stand or fall together as argued below. Claims 29-35 are dependent upon claim 28. (Henceforth claim 28 and those claims that depend from claim 28 shall be referred to as “Group D”). All claims of Group D stand or fall together as argued below. Groups B, C, and D stand or fall together as argued below.

## **Brief Review of the References**

Baldwin (U.S. Patent No. 6,025,853) relates to a processing chip that uses a deep pipeline of multiple asynchronous units to achieve a high net throughput in 3D rendering.<sup>1</sup>

Brent et al. (U.S. Patent No. 5,459,864) relates to automatic load balancing among plural queue processors, automatic recovery from any failing queue processor, and automatic reconfiguration for the 20 subsystem containing the processors, while the subsystem continues to control data movement within or between electronic storage media without intervention from the operating system.<sup>2</sup>

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<sup>1</sup> United States Patent 6,025,853, col. 1, lines 6-8

<sup>2</sup> United States Patent 5,459,864, col. 1, lines 18-24

## ARGUMENT

**Issue: Are claims 1, 3-5 and 7-35 unpatentable over Baldwin (6,025,853) in view of Brent et al (5,459,864) under 35 U.S.C. 103(a)?**

### **Requirements for Rejection under 35 USC 103(a)**

A fundamental notion of patent law is the concept that invention lies in the new combination of old elements. Therefore, a rule that every invention could be rejected as obvious by merely locating each element of the invention in the prior art and combining the references to formulate an obviousness rejection is inconsistent with the very nature of "invention." Consequently, a rule exists that a combination of references made to establish a *prima facie* case of obviousness must be supported by some teaching, suggestion, or incentive contained in the prior art which would have led one of ordinary skill in the art to make the claimed invention.

The inquiry is not whether each element existed in the prior art, but whether the invention as a whole is obvious in light of the prior art. *Hartness International, Inc. v. Simplimatic Engineering Co.*, 819 F.2d 100, 2 U.S.P.Q.2d 1826 (Fed. Cir. 1987). The examiner bears the burden of establishing a *prima facie* case of obviousness based on the prior art when rejecting claims under 35 U.S.C. § 103. *In re Fritch*, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992).

**Overview of the Rejection under 35 USC 103(a)**

Claims in groups A, B, C, and D all stand rejected under 35 USC Section 103(a) as being unpatentable over *Baldwin* in view of *Brent et al.* For the purpose of clarity, the independent claim of each group is reproduced below.

Claim 1, representative of Group “A” are dependant, is reproduced below.

A graphics processor, comprising:

- a plurality of paralleled graphics computational units; and
- one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units.

Claim 12, representative of Groups “B”, “C”, and “D” is reproduced below.

A method of 3D graphics rendering, comprising the actions of:

- providing a plurality of parallellized graphics computational units;
- bypassing defective ones of said units, and
- distributing incoming tasks only among operative ones of said units.

**I. The combination of the cited references do not teach or suggest all limitations of the claims of Groups A, B, C or D.**

The combination of the Baldwin and Brent references do not teach or suggest all limitations of, for example, claim 1. Claim 1 claims in part “a plurality of paralleled graphics computational units” which is part of a single processor. Brent’s teaching deals with the allocation between separate processors, while Baldwin deals with the allocation within a single processor. As argued below, the combination of the Brent and Baldwin references does not teach or suggest a single processor with the limitations of claim 1.

As determined in *Thrift*,<sup>3</sup> a rejection which “does not discuss the unique limitations” of the claims was held to be “simply inadequate on its face.” In this case, a rejection was held “not supported by substantial evidence because the cited references do not support each limitation of claim 11.” See *In re Vaeck*, 947 F.2d 488, 493, 20 USPQ2d 1438, 1443 (Fed. Cir. 1991).<sup>4</sup> In the present case, the examiner has failed to address the unique limitations of *a graphics processor ... with one or more task allocation units programmed to bypass defective ones of said units*. Therefore, a prima facie case of obviousness has not been established by the Examiner.

Claim Groups A, B, C, and D all are directed towards a processor with “A single processor, with parallel functions” that was previously pictured in the original application as follows:

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<sup>3</sup> *In re Thrift*, 298 F.3d 1357 (Fed.Cir. 2002).

<sup>4</sup> *In re Thrift*, 298 F.3d at 1366 (emphasis added).

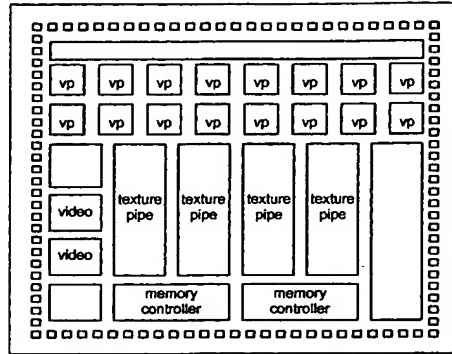
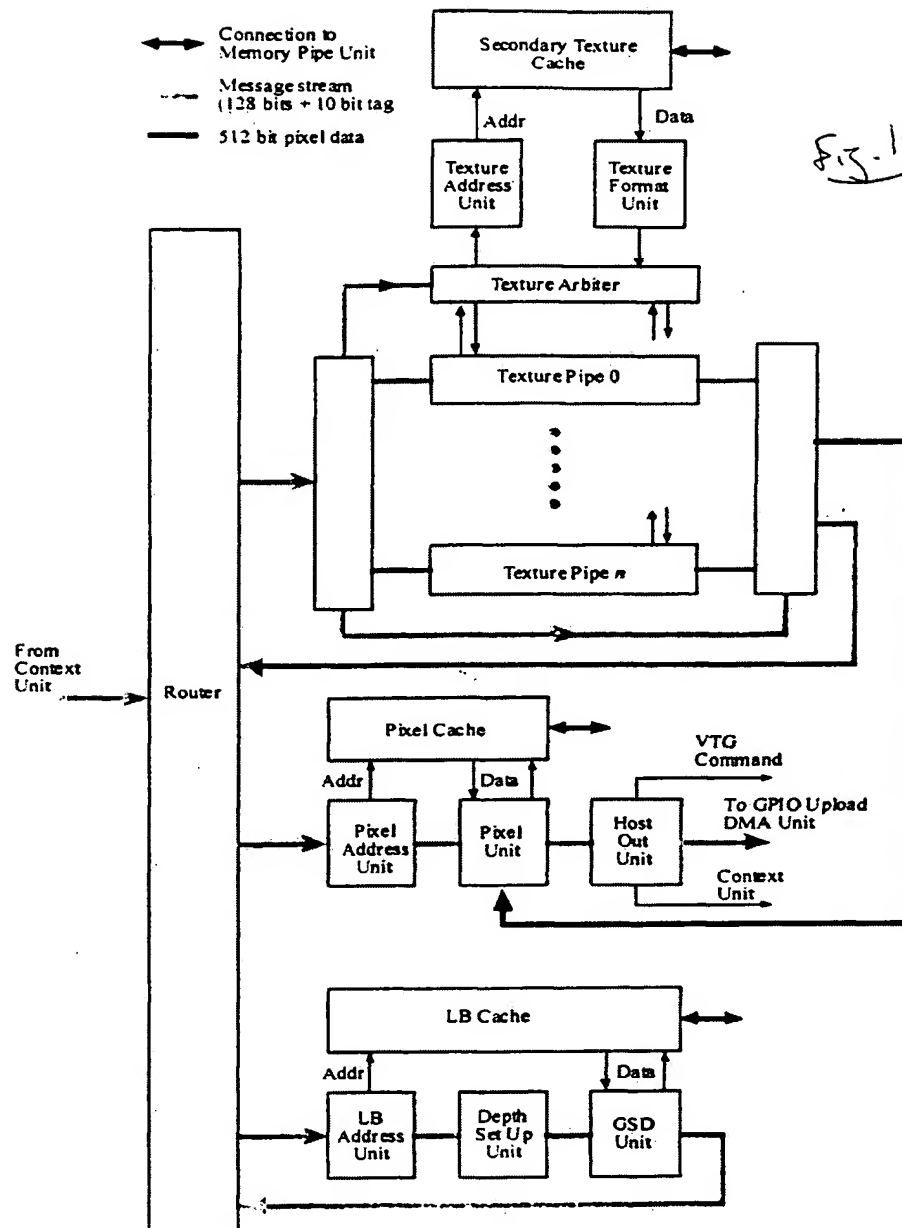


FIG. 1

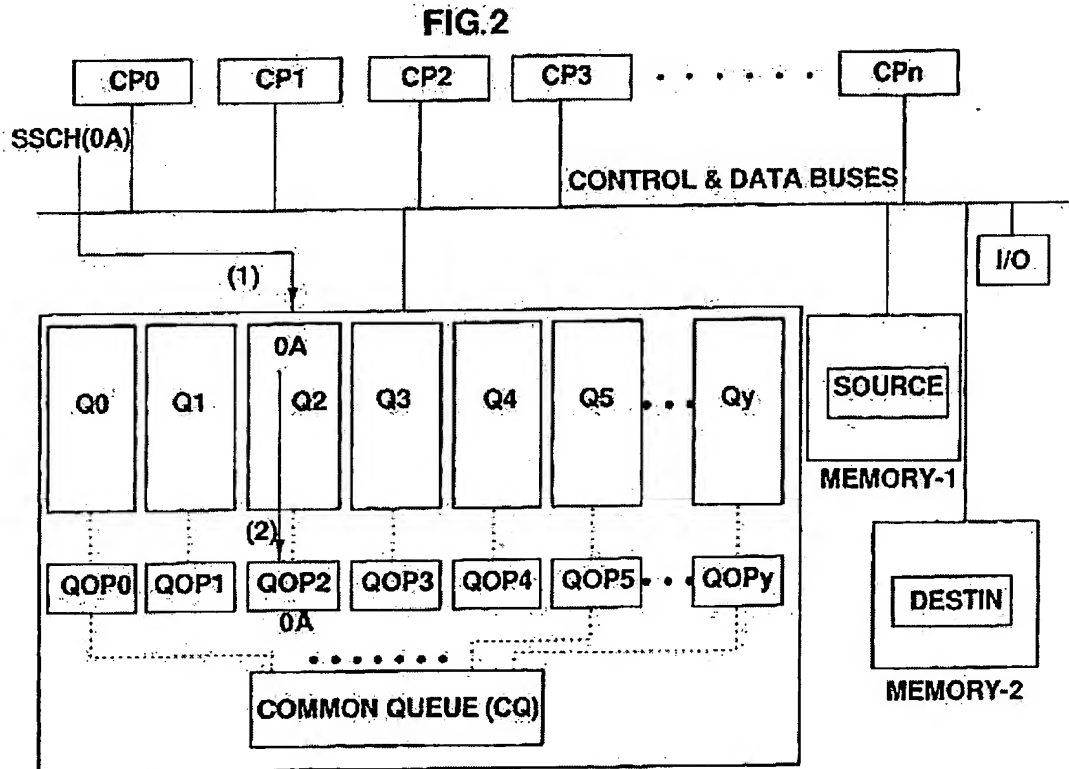
As illustrated, this single processor is a die component that is comprised of several texture pipes controlled by an internal task allocation unit.

The way that this processor controls data was shown in figure 1B. This figure illustrates the “a plurality of parallellized graphics computational units” as shown by Texture Pipe 0 through Texture Pipe N. The “task allocation units” are shown in the “Router” function which enables the processor to bypass defective Texture Pipes. It is the Router unit that, in this embodiment, allows the processor to bypass a defective pipeline within the processor.



In contrast, the prior art teaches away from the present inventions as it not only operates on a completely different scale, but also requires a plurality of processors in order to function. The Brent patent requires a multiple of separate, fully functional processors in order to function. This is the "**PLURAL QUEUE**"

**PROCESSORS**” requirement that is named in Brent application. Figure 2 of the Brent patent illustrates this, and is reproduced below:



The entire present application would be placed within any one of the CP0, CP1, etc. elements within the Figure 2 of the Brent Application. In the prior art if a cpu were to fail, it would be eliminated completely from the system. The Brent solution to a failed pipeline is to disable the entire processor, whereas in the present invention the solution is to disable only the pipeline leaving the remainder of the processor to function. The Brent solution is like amputating a limb in the case of a broken artery in order to save the body, wherein the present application can close the artery and save the limb.



If the prior art cited references were combined, they would only create an extension of the Brent reference. This would not allow for the disabling of a partially defective processor, and would require the removal of an entire processor unit.

Moreover, in the '864 patent the processor failure must occur while the processor is running, wherein the current invention a diagnostic can be preformed to detect the error, and the failure can be prevented prior to the processor even leaving the factory. This feature was also noted in the original application.

“To allow this to be implemented we need to have reconfigurability in the architecture, independent scan chains so that a manufacturing fault can be isolated and a method of recording the test result inside the chip.”<sup>5</sup>

This is another good example of the differences between the present inventions which can prevent failure even when there is a faulty component, and the prior art which teaches simply to disable the entire component.

The only way that the examiner can reach the present invention is by making significant modifications to the cited references. The mere fact that a prior art reference can be readily modified does not make the modification obvious unless the prior art suggested the desirability of the modification. In re Laskowski, 871 F.2d 115, 10 U.S.P.Q.2d 1397 (Fed. Cir. 1989) and also see In re Fritch, 972 F.2d 1260, 23 U.S.P.Q.2d 1780 (Fed. Cir. 1992) and In re Mills, 916 F.2d 680, 16 U.S.P.Q.2d 1430 (Fed. Cir. 1993). The examiner may not merely state that the modification would have been obvious to one of ordinary skill in the art without pointing out in the prior art a suggestion of the desirability of the proposed modification.

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<sup>5</sup> Page 3, Lines 23-25, of the Original Application, Atty Docket TD-168

In the present case, Examiner has neither suggested the necessary modifications, nor has pointed to any suggestion in the references to make such modifications.

Therefore, the combination of the Baldwin and Brent references do not teach or suggest all limitations of, for example, claim 1. As previously stated, claim 1 claims in part “a plurality of paralleled graphics computational units” which is part of a single processor. Brent’s teaching deals with the allocation between separate processors, while Baldwin deals with the allocation between units of a single processor. Even if properly combined, these references together do not teach all of the limitations of claim 1. Hence, the combination of the Brent and Baldwin references do not teach or suggest a single processor with the limitations of claim 1, or the other inventions disclosed by the applicant. This argument applies equally to all claim groups, including Groups A, B, C, and D.

## **II. There Is No Teaching or Suggestion In The Cited References To Combine The Cited References**

There is no teaching or suggestion to combine the cited references to form the inventions found in Group A, B, C or D. In determining obviousness, an applicant's teachings may not be read into the prior art. *Panduit Corp. v. Denison Mfg. Co.*, 810 F.2d 1561, 1575 n. 29, 1 U.S.P.Q. 1593, 1602 n. 29 (Fed. Cir. 1987) (citing need to "guard against hindsight and the temptation to read the inventor's teachings into the prior art"). A determination of the desirability of combining prior art references must be made without the benefit of hindsight afforded by an applicant's disclosure. *In re Paulsen*, 30 F.3d 1475, 1482, 31 U.S.P.Q. 1671, 1676 (Fed. Cir. 1994).

Applicants aver that examiner could not have reached the proposed combination without using the present invention as a template. This is an impermissible use of hindsight.

Examiner Tung writes in his rejection that:

*“Brent teaches a load balancing, error recovery and reconfiguration control in a data movement subsystem with cooperating plural queue processors (Fig. 2, abstract, col. 2, lines 39-45, col. 5, lines 49-52 and col. 6, lines 11-18). It would have been obvious to one of ordinary skill in the art at the time the present invention was made to combine the teachings of bypass defective unit and distribute load from defective unit to other units of Brent into the system of Baldwin in order to automatic load balancing among plural processors, automatic recovery from any failing processor, and automatic reconfiguration for the subsystem containing the processors without intervention from the operating system as taught by Brent (col. 1, lines 18-24). Therefore, at least claims 1, 3-5 and 7 would have been obvious<sup>6</sup>.”*

This assertion that it is obvious to combine the prior art is flawed for at least two reasons. First, the ‘864 requires “plural queue processors”<sup>7</sup> in order to recover from any “failing queue processor”<sup>8</sup>. The ‘864 is designed to recover from a fatal error in a multi-processor environment. The present invention is designed to actively disable a section of an otherwise defective processor in order to make it functional. This was highlighted in the following passage from the original application:

*“During testing a single bit error anywhere on the die will force that die to be scrapped... However, by internally reconfiguring the chip we can still make use of a die with one or more failing texture pipes, for example. This allows us to take die which would otherwise be classified as scrap and use them in a lower performance product.”<sup>9</sup>*

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<sup>6</sup> Id.

<sup>7</sup> US Patent 5,459,864, Col 1, line 18-20.

<sup>8</sup> Id.

<sup>9</sup> Page 3, Lines 15-22, of the Original Application, Atty Docket TD-168.

The '864, when encountering an error within a queue processor, reconfigures to avoid the failed processor – including shutting down possibly operable pipelines. The patent states this point in the following passage:

*“...the failing processor is stopped, removed from the operational sub- 50 system, and its work redistributed to other processors through the subsystem workload balancing process.”<sup>10</sup>*

The relevant cited prior art only applies when a total processor failure occurs, whereas the present application prevents the processor failure by preemptively removing defective pipelines thereby allowing the processor to function. In the event of a processor failure, the '864 patent requires that “the failing processor is stopped, removed from the operational subsystem”<sup>11</sup>, whereas in the present inventions allow for “use partially defective die as fully functioning parts with lower performance”<sup>12</sup>

Thus, the teachings of the Baldwin and Brent references are clearly incompatible, because they apply to difference scales – Baldwin deals with incompatible units at a single processor, while Brent deals with separate, individual processors and does not address computational unit is within those processors.

The second reason that it is not obvious to combine the cited reference is that there is no statement, method, or suggestion in those references for such a combination. No such statement, motive, or suggestion is found in the references.

A proper *prima facie* case of obviousness cannot be established by combining the teachings of the prior art absent some teaching, incentive, or suggestion supporting the

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<sup>10</sup> US Patent 5,459,864, Col 5, line 47-52.

<sup>11</sup> US Patent 5,459,864, Col 5, line 48-52.

<sup>12</sup> Page 4, Lines 3-5, of the Original Application, Atty Docket TD-168.

combination. *In re Napier*, 55 F.3d 610, 613, 34 U.S.P.Q.2d 1782, 1784 (Fed. Cir. 1995); *In re Bond*, 910 F.2d 831, 834, 15 U.S.P.Q.2d 1566, 1568 (Fed. Cir. 1990).

Therefore, the cited references are not properly combinable because there is no statement, motive, or suggestion to make the combination.

### **III. The Cited References Cannot be Properly Combined as the Examiner suggests.**

As argued above, Brent deals with the allocation of tasks between multiple processors, while Baldwin deals with the allocation of tasks within a single processor. The difference in the magnitude of scale is made more clear below.

#### **A. The cited references cannot be combined to form the inventions found in Group A.**

The asserted combination of references does not support each limitation of the independent claim found in Group A. Specifically, Claim 1 recites “**a plurality of paralleled graphics computational units; and one or more task allocation units programmed to bypass defective ones of said units within said groups, and to distribute incoming tasks only among operative ones of said units.**”

Examiner Tung begins his rejection of Group A under 103(a) by pointing out that “*Baldwin fails to explicitly teach or suggest one or more task allocation units*

*programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits.*<sup>13</sup>”

This admission, that the Baldwin art fails to teach the distribution of tasks when a processor has a defective pipeline, highlights one of the differences between the prior art and the present inventions that teaches “*graphics processor, comprising a plurality of parallelled graphics computational units and one or more task allocation units programmed to bypass defective ones of said units.*” The Baldwin reference requires that all parallel subunits function properly whereas in the present inventions the processor will continue to function, albeit at a reduced capacity, by disabling a subunit.

Examiner Tung attempts to cure this defect by applying the *Brent et al* reference. However, *Brent et al.* does not disclose or suggest one or more task allocation units to bypass defective graphics computational units and to distribute incoming tasks only among operative graphics computational units. The Examiner has correctly noted that *Brent et al.* teaches a load balancing, error recovery and reconfiguration control in a *data movement subsystem with cooperating plural queue processors*. Brent does not teach a process by which a single processor may continue to function even though it is partially defective. There is no suggestion to use a partially operative single processor in any of the cited prior art. Instead, Brent teaches away from this innovation because in order to function it requires a processor that is partially defective to be completely disabled, whereas in the present inventions, the partially operable processor is allowed to continue to function within a system. Using out invention as a template is an impermissible use of hindsight.

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<sup>13</sup> Page 2 of the office action dated August 5, 2005

*A System using “plural queue processors” to compensate for the failure of a graphics processor does not teach or suggest “A graphics processor with one or more task allocation units programmed to bypass defective ones.”*

There is a delineation that needs to be made between the example the Examiner Tung alludes to wherein there is a plurality of queue processors, and the present invention wherein **A GRAPHICS PROCESSOR WITH ONE OR MORE TASK ALLOCATION UNITS PROGRAMMED TO BYPASS DEFECTIVE ONES.**

In the rejection of the claims, Examiner Tung asserts that: *“It is old and well known and well used in the art to dynamically load balanced among multiple processors include skip or bypass defective unit(s)”<sup>14</sup>.*

This application deals with the ability to bypass a defective pipeline within a SINGLE processor (“A GRAPHICS PROCESSOR”) as opposed to the MULTIPLE (“PLURAL QUEUE PROCESSORS”) processors alluded to in the prior art.

Therefore, the examiner has failed to show that the cited references are capable of being properly combined. Moreover, even if the examiner can show that such a combination is possible, a position that the applicant strongly disagrees with, the combination of such cited references would lead to an invention directed towards a system of multiple processors rather than the single processor solution disclosed by the inventor.

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<sup>14</sup> id.

**B. The cited references cannot be combined to form the inventions found in Groups B,C, and D.**

Examiner does not individually address the inventions in Group B, C, or D in his rejection, and instead reiterates the arguments he has made to his rejection of Group A. Just as the recited references cannot be combined to for the inventions found in Group A, the references cannot be combined to form the inventions found in Group B, C, or D.

The independent claim of Group B reads **“A method of 3D graphics rendering, comprising the actions of providing a plurality of parallellized graphics computational units; bypassing defective ones of said units, and distributing incoming tasks only among operative ones of said units.”** There is no background in the prior art to have a graphics processor with multiple graphics computational units within the single processor, where there can be the bypassing of some of the units during operation.

Claim 20, from which all claims in Group “C” depend, claims the inventions of a computer graphics system comprising means for providing a plurality of parallellized graphics computational units means for bypassing defective ones of said units, and means for distributing incoming tasks only among operative ones of said units. Again, there is no background in the prior art to have a graphics processor with multiple graphics computational units within the single processor, where there can be the bypassing of some of the units during operation.

Claim 28, from which all claims in Group “D” depend, claims a method for computer graphics system operation, comprising the actions of providing a plurality of parallellized rendering units bypassing defective ones of said units, and distributing incoming tasks only among operative ones of said units. Again, there is no background in the prior art to have a graphics processor with multiple graphics computational units within



the single processor, where there can be the bypassing of some of the units during operation.

The specification clearly states that each one of these computational units are subparts of a single processor unit. The original specification discloses this innovative feature when it states “A graphics processor, comprising: a plurality of parallellized graphics computational units”<sup>15</sup> Examiner Tung has applied his rejection to claim continues in his rejection to correctly points out that “*Baldwin fails to explicitly teach or suggest one or more task allocation units programmed to bypass defective ones of said subunits within said groups, and distribute incoming tasks only among operative ones of said subunits.*”<sup>16</sup>,

This admission, that the Baldwin art fails to teach the distribution of tasks when a processor has a defective pipeline, highlights one of the differences from the present inventions that teaches “*graphics processor, comprising a plurality of parallelled graphics computational units and one or more task allocation units programmed to bypass defective ones of said units.*” The Baldwin reference requires that all parallel subunits function properly whereas in the present inventions the processor will continue to function, albeit at a reduced capacity, by disabling a subunit.

Examiner Tung attempts to cure this defect by applying the *Brent et al* reference. However, *Brent et al.* does not disclose or suggest one or more task allocation units to bypass defective graphics computational units and to distribute incoming tasks only among operative graphics computational units. The Examiner has correctly noted that *Brent et al.* teaches a load balancing, error recovery and reconfiguration control in a *data movement*

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<sup>15</sup> Page 44, Lines 14-15, of the Original Application, Atty Docket TD-168.

<sup>16</sup> Page 2 of the office action dated August 5, 2005

*subsystem with cooperating plural queue processors*. Brent does not teach a process by which a single processor may continue to function even though it is partially defective. There is no suggestion to use a partially operative processor. Instead, Brent teaches away from this innovation and it requires a processor that is partially defective to be disabled within a system.

Therefore, the examiner has failed to show that the cited references are capable of being properly combined. Moreover, even if the examiner can show that such a combination is possible, a position that the applicant strongly disagrees with, the combination of such cited references would lead to an invention directed towards a system of multiple processors rather than the single processor solution disclosed by the inventor.


Therefore, for all of the above reasons, applicants respectfully submit that Examiner has failed to make out a *prima facie* case of obviousness.

### **Requested Relief**

For the reasons advanced above, Appellant respectfully contends that claims 1, 3-5 and 7-35 are patentable. Therefore, reversal of this rejection is respectfully requested.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection of this paper, including extension of time fees, to Deposit Account 07-2320 and please credit any excess fees to such deposit account.

Respectfully submitted,

A handwritten signature in black ink, appearing to read 'D. W. Roe', written in a cursive style.

David W. Roe

Reg.No. 55,785

Attorney for Appellant

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: :  
Kent : Art Unit: 2676  
AN 10/086,980 : Examiner: Tung, Kee M.  
Filed: 03/01/2002 : Atty's Docket: TD-168

For: Yield Enhancement of Complex Chips (confirmation no. 6304)

**APPENDIX A – Text of Claims on Appeal**

**IN THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. A graphics processor, comprising:  
a plurality of parallellized graphics computational units; and  
one or more task allocation units programmed to bypass defective ones of said units within said  
groups, and to distribute incoming tasks only among operative ones of said units.
2. (canceled)
3. The graphics processor of claim 1, wherein each of said parallellized graphics computational units also  
includes respective multiple vertex processors.
4. The graphics processor of claim 1, wherein each of said parallellized graphics computational units also  
includes respective texturing pipelines.
5. The graphics processor of claim 1, wherein each of said parallellized graphics computational units also  
includes a respective memory controller.
6. (canceled)
7. A method of 3D graphics rendering which comprises: using a task allocation unit and parallellized graphics  
computational units with relations as recited in claim 1.

8. The graphics processor of claim 1, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.
9. The graphics processor of claim 1, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.
10. The graphics processor of claim 4, wherein said texturing pipelines also include a shading unit and a texture filter unit.
11. The graphics processor of claim 4, wherein said texturing pipelines also include a shading unit and a primary texture cache.
12. A method of 3D graphics rendering, comprising the actions of:
  - providing a plurality of parallellized graphics computational units;
  - bypassing defective ones of said units, and
  - distributing incoming tasks only among operative ones of said units.
13. The method of claim 12, wherein each of said parallellized graphics computational units also includes respective multiple vertex processors.
14. The method of claim 12, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.
15. The method of claim 12, wherein each of said parallellized graphics computational units also includes respective multiple texturing pipelines.
16. The method of claim 12, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.

17. The method of claim 12, wherein each of said parallellized graphics computational units also includes a respective memory controller.

18. The method of claim 15, wherein said texturing pipelines also include a shading unit and a texture filter unit.

19. The method of claim 15, wherein said texturing pipelines also include a shading unit and a primary texture cache.

20. A computer graphics system comprising:

means for providing a plurality of parallellized graphics computational units;

means for bypassing defective ones of said units, and

means for distributing incoming tasks only among operative ones of said units.

21. The system of claim 20, wherein each of said parallellized graphics computational units also includes respective multiple vertex processors.

22. The system of claim 20, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative vertex processors.

23. The system of claim 20, wherein each of said parallellized graphics computational units also includes respective multiple texturing pipelines.

24. The system of claim 20, wherein one or more of said parallellized graphics computational units operate with no more than 4 operative texturing pipelines.

25. The system of claim 20, wherein each of said parallellized graphics computational units also includes a respective memory controller.

26. The system of claim 23, wherein said texturing pipelines also include a shading unit and a texture filter unit.

27. The system of claim 23, wherein said texturing pipelines also include a shading unit and a primary texture cache.

28. A method for computer graphics system operation, comprising the actions of:  
    providing a plurality of parallellized rendering units;  
    bypassing defective ones of said units, and  
    distributing incoming tasks only among operative ones of said units.

29. The method of claim 28, wherein each of said parallellized rendering units also includes respective multiple vertex processors.

30. The method of claim 28, wherein one or more of said parallellized rendering units operate with no more than 4 operative vertex processors.

31. The method of claim 28, wherein each of said parallellized rendering units also includes respective multiple texturing pipelines.

32. The method of claim 28, wherein one or more of said parallellized rendering units operate with no more than 4 operative texturing pipelines.

33. The method of claim 28, wherein each of said parallellized rendering units also includes a respective memory controller.

34. The method of claim 31, wherein said texturing pipelines also include a shading unit and a texture filter unit.

35. The method of claim 31, wherein said texturing pipelines also include a shading unit and a primary texture cache.

## **APPENDIX B – Copy of Cited References**




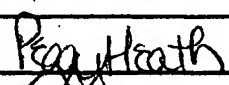
**APPENDIX C – Copy of Notice of Appeal previously filed**

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

<b>TRANSMITTAL FORM</b>  (to be used for all correspondence after initial filing)	Application Number	10/086,980	
	Filing Date	03/01/2002	
	First Named Inventor	Kent	
	Art Unit	2576	
	Examiner Name		
Total Number of Pages in This Submission	3	Attorney Docket Number	TD-168

ENCLOSURES (Check all that apply)		
<input type="checkbox"/> Fee Transmittal Form <input type="checkbox"/> Fee Attached  <input type="checkbox"/> Amendment/Reply <input type="checkbox"/> After Final <input type="checkbox"/> Affidavits/declaration(s)  <input type="checkbox"/> Extension of Time Request <input type="checkbox"/> Express Abandonment Request <input type="checkbox"/> Information Disclosure Statement  <input type="checkbox"/> Certified Copy of Priority Document(s)  <input type="checkbox"/> Reply to Missing Parts/ Incomplete Application <input type="checkbox"/> Reply to Missing Parts under 37 CFR 1.52 or 1.53	<input type="checkbox"/> Drawing(s) <input type="checkbox"/> Licensing-related Papers  <input type="checkbox"/> Petition <input type="checkbox"/> Petition to Convert to a Provisional Application <input type="checkbox"/> Power of Attorney, Revocation Change of Correspondence Address  <input type="checkbox"/> Terminal Disclaimer  <input type="checkbox"/> Request for Refund  <input type="checkbox"/> CD, Number of CD(s) _____ <input type="checkbox"/> Landscape Table on CD	<input type="checkbox"/> After Allowance Communication to TC  <input type="checkbox"/> Appeal Communication to Board of Appeals and Interferences  <input checked="" type="checkbox"/> Appeal Communication to TC (Appeal Notice, Brief, Reply Brief)  <input type="checkbox"/> Proprietary Information  <input type="checkbox"/> Status Letter  <input type="checkbox"/> Other Enclosure(s) (please identify below):
Remarks		

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT			
Firm Name	Groover & Holmes		
Signature			
Printed name	N. Elizabeth Pham		
Date	01/04/2005	Reg. No.	49,042

CERTIFICATE OF TRANSMISSION/MAILING			
I hereby certify that this correspondence is being facsimile transmitted to the USPTO or deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below:			
Signature			
Typed or printed name	Peggy Heath	Date	01/04/2005

This collection of information is required by 37 CFR 1.5. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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PTO/SB/31 (09-04)  
Approved for use through 07/31/2008. OMB 0651-0031  
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

NOTICE OF APPEAL FROM THE EXAMINER TO THE BOARD OF PATENT APPEALS AND INTERFERENCES		Docket Number (Optional) <u>T0-168</u>	
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on <u>January 4, 2005</u>		In re Application of <u>Kent</u>	
Signature <u>Peggy Heath</u>		Application Number <u>101086980</u>	Filed <u>03/01/2002</u>
Typed or printed name <u>PEGGY HEATH</u>		For <u>Yield enhancement of Complex Chips</u>	Art Unit <u>2676</u>
Examiner			
Applicant hereby appeals to the Board of Patent Appeals and Interferences from the last decision of the examiner.			
The fee for this Notice of Appeal is (37 CFR 41.20(b)(1))		\$ <u>500.00</u>	
<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27. Therefore, the fee shown above is reduced by half, and the resulting fee is:		\$ _____	
<input type="checkbox"/> A check in the amount of the fee is enclosed.			
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached.			
<input type="checkbox"/> The Director has already been authorized to charge fees in this application to a Deposit Account. I have enclosed a duplicate copy of this sheet.			
<input checked="" type="checkbox"/> The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. <u>07-2320</u> . I have enclosed a duplicate copy of this sheet.			
<input type="checkbox"/> A petition for an extension of time under 37 CFR 1.136(a) (PTO/SB/22) is enclosed.			
<b>WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.</b>			
I am the		<u>N. Elizabeth Pham</u> Signature	
<input type="checkbox"/> applicant/inventor.		<u>N. Elizabeth Pham</u> Typed or printed name	
<input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/98)			
<input checked="" type="checkbox"/> attorney or agent of record. Registration number <u>49,042</u>		<u>972-980-5840</u> Telephone number	
<input type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34. _____		<u>1-4-05</u> Date	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below.			
<input checked="" type="checkbox"/> Total of <u>2</u> forms are submitted.			

This collection of information is required by 37 CFR 41.31. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

**APPENDIX D– Copy of Application Drawings**

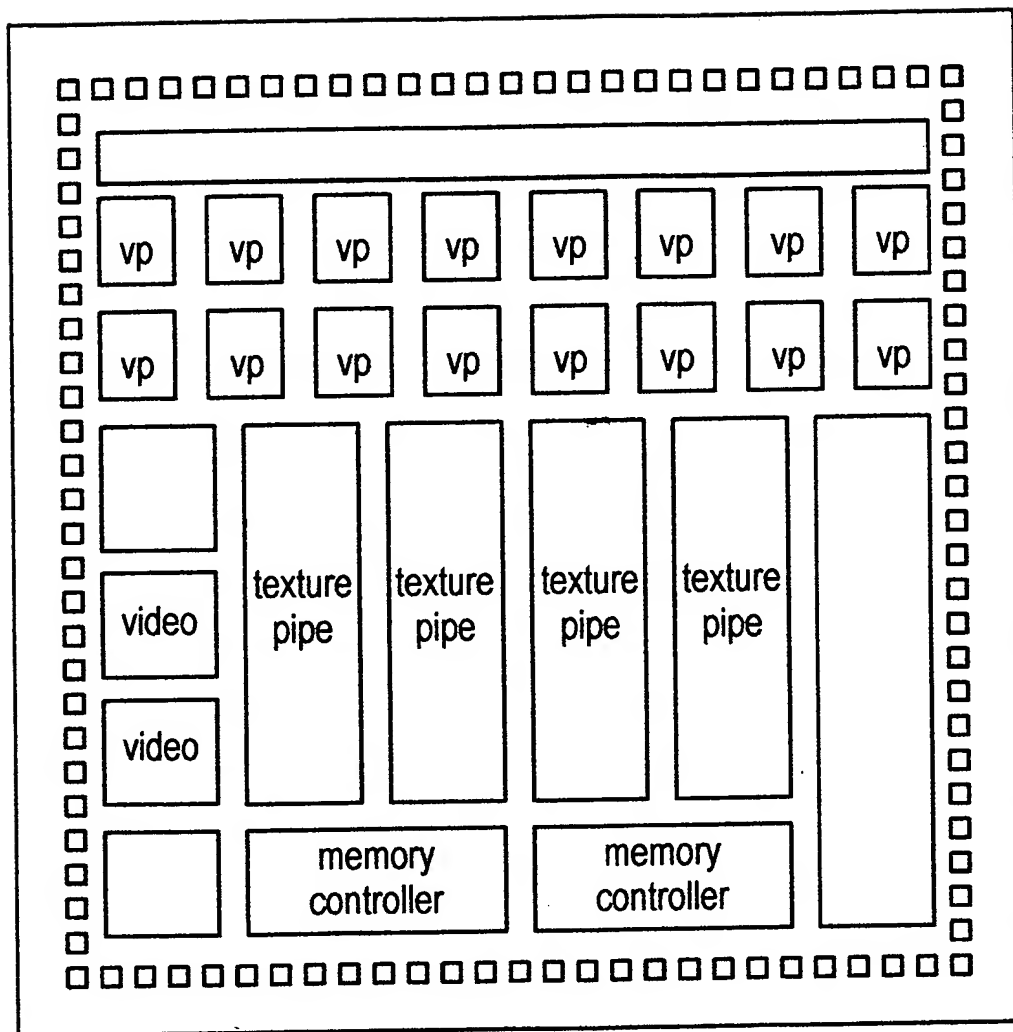


FIG. 1

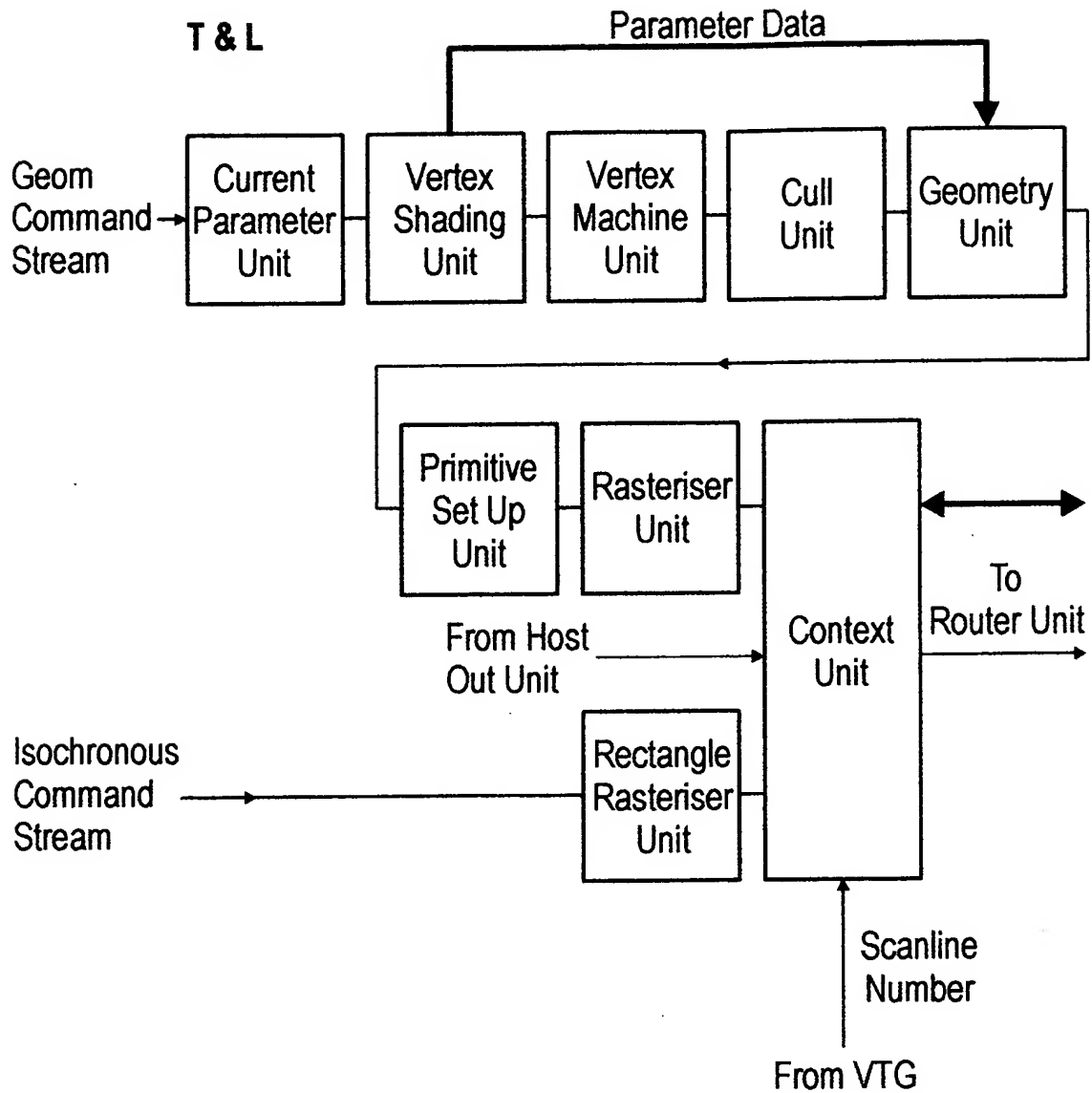


FIG. 1A

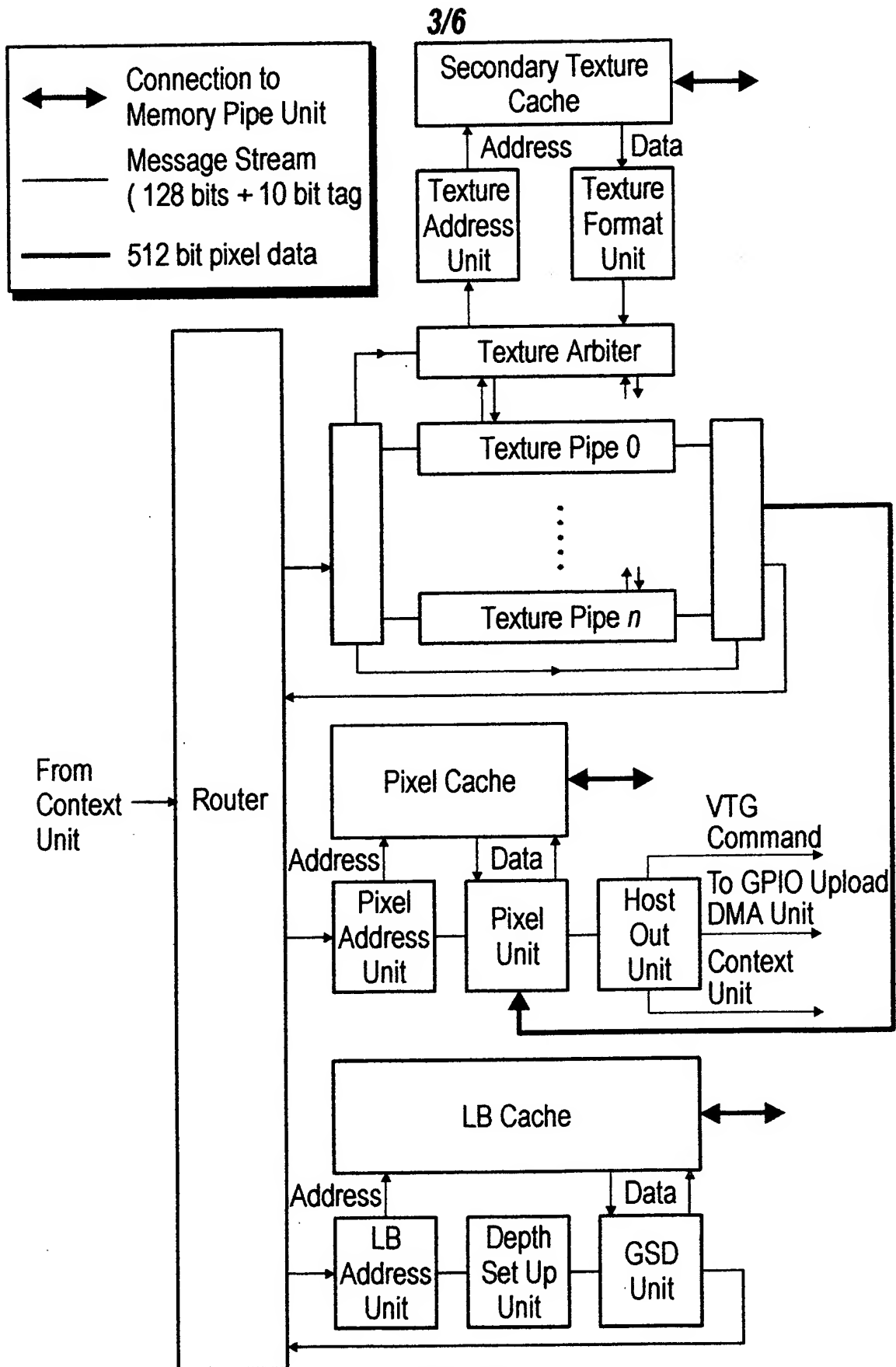


FIG. 1B

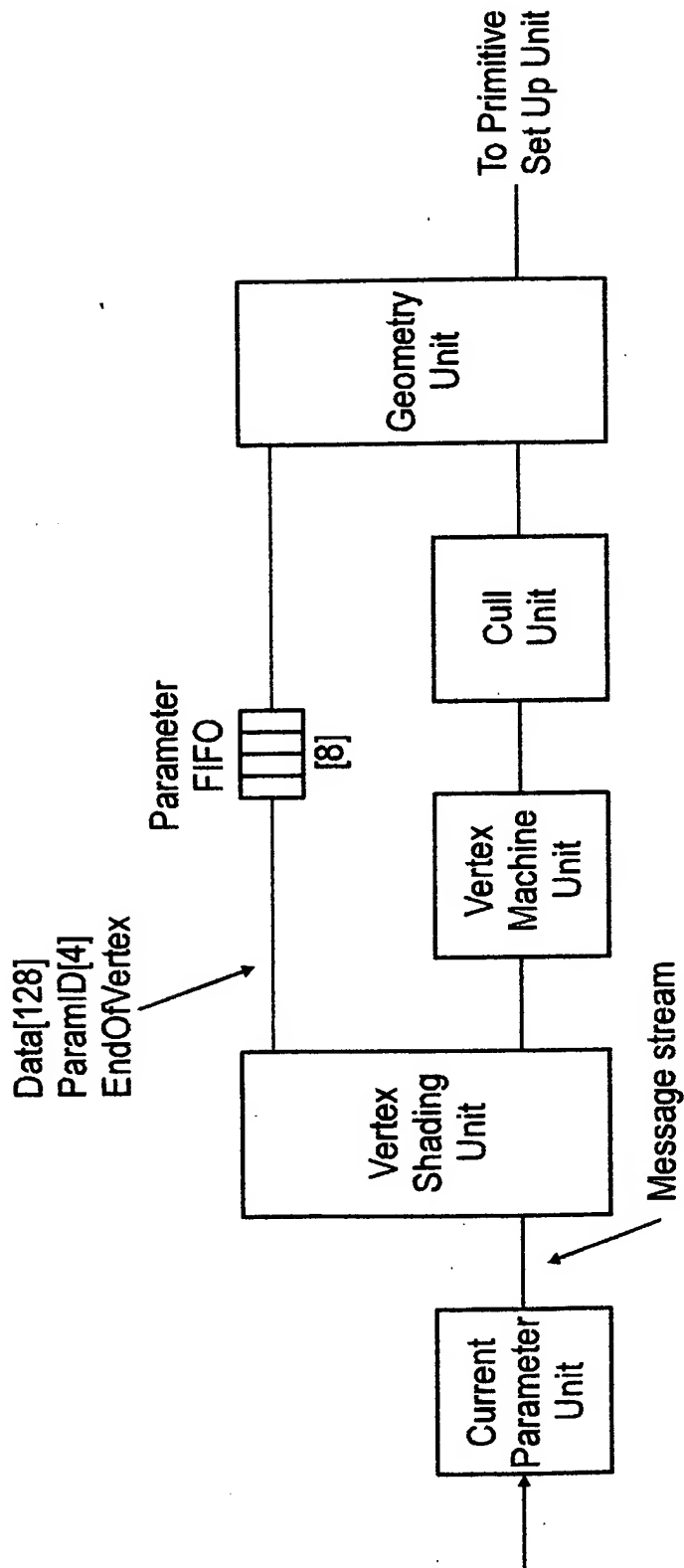


FIG. 1C



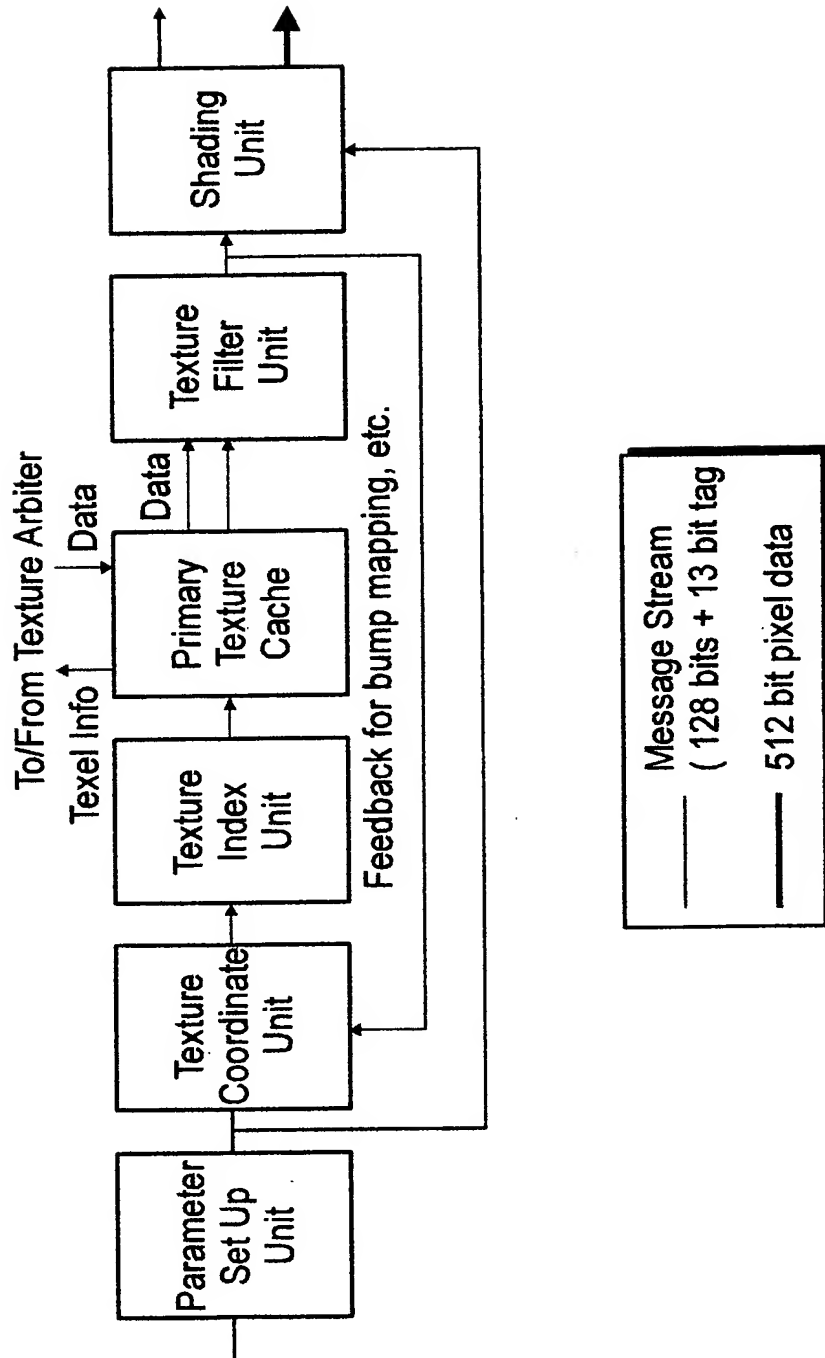


FIG. 1D

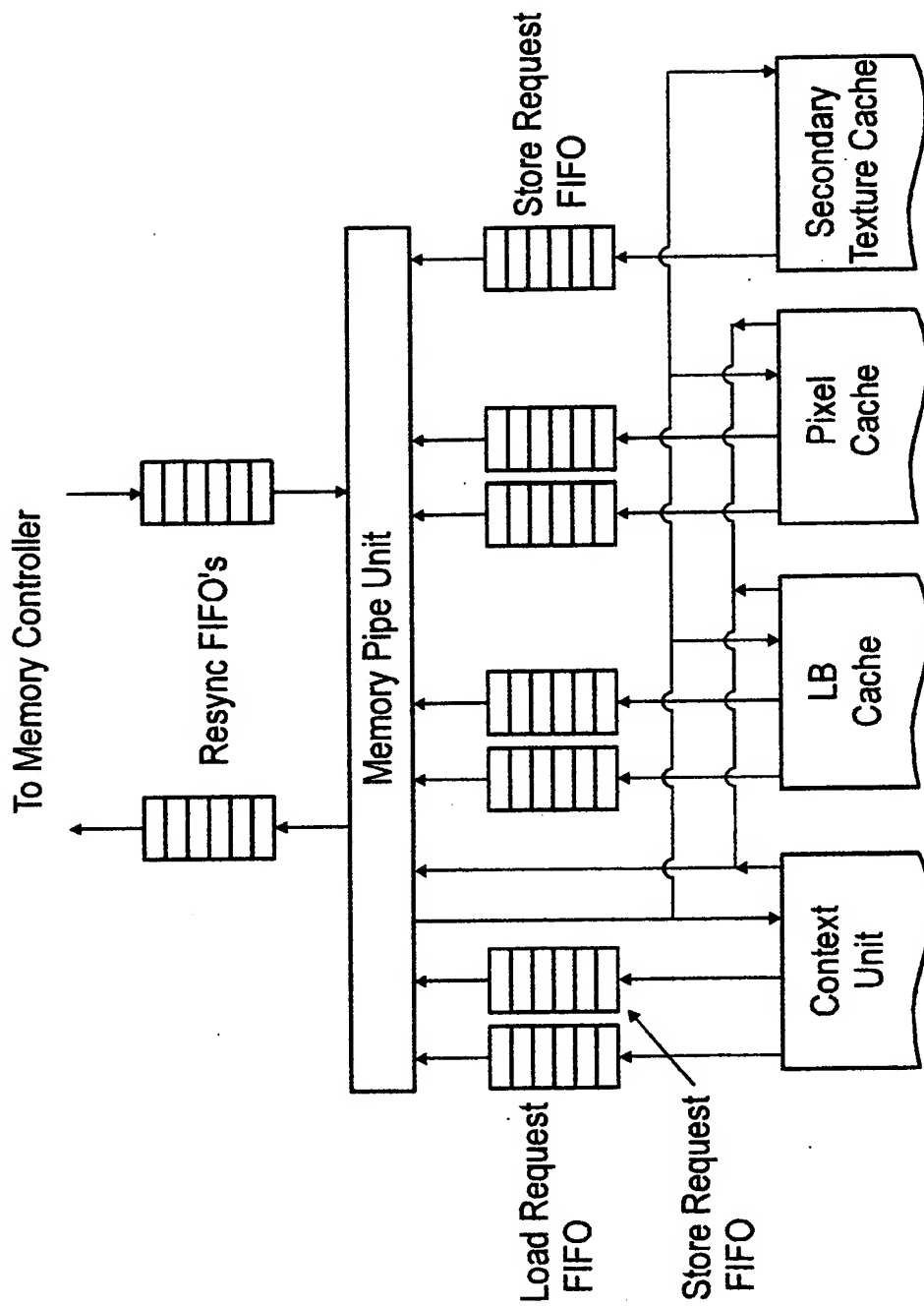


FIG. 1E